In the claims:

Please substitute the following full listing of claims for the claims as originally filed or most recently amended. Claims 1 and 5 have been cancelled without prejudice of disclaimer and claims 2 and 3, which have been indicated to be allowable but objected to as depending from a rejected claim have been rewritten in independent form and dependency of other claims has been revised accordingly. New claims 17 and 18, identical to claims 9 and 10 but depending from claim 3 have been added.

1. (Cancelled)

2. (Currently Amended) An integrated circuit including

a patterned copper layer,

a patterned aluminum layer,

an opening in a layer of material, said opening extending between a location on said patterned copper layer and a location on said patterned aluminum layer,

a multi-layer barrier liner in said opening and having a thickness, said barrier liner extending between said patterned aluminum layer and said patterned copper layer at said location on said patterned copper layer and across said copper layer to cover a bottom of said opening, said multi-layer barrier layer including at least a first layer being of a material which is conductive and having adhesion to copper and tungsten comparable to that of tantalum or tantalum nitride or titanium nitride and resisting interdiffusion of copper and tungsten and a second layer formed on said first layer and being of a material which assists in the formation of a stud during deposition of tungsten on which tungsten can be deposited, one or both of said first and second layers forming a conductive barrier to process materials which

are reactive with copper, and

a stud connection formed of tungsten and located within said barrier liner ~~An integrated circuit as recited in claim 1~~ wherein said barrier liner comprises

a layer of tantalum nitride, and

a layer of PVD tungsten.

3. (Currently Amended) An integrated circuit including

a patterned copper layer,

a patterned aluminum layer,

an opening in a layer of material, said opening extending between a location on said patterned copper layer and a location on said patterned aluminum layer,

a multi-layer barrier liner in said opening and having a thickness, said barrier liner extending between said patterned aluminum layer and said patterned copper layer at said location on said patterned copper layer and across said copper layer to cover a bottom of said opening, said multi-layer barrier layer including at least a first layer being of a material which is conductive and having adhesion to copper and tungsten comparable to that of tantalum or tantalum nitride or titanium nitride and resisting interdiffusion of copper and tungsten and a second layer formed on said first layer and being of a material which assists in the formation of a stud during deposition of tungsten on which tungsten can be deposited, one or both of said first and second layers forming a conductive barrier to process materials which are reactive with copper, and

a stud connection formed of tungsten and located within said barrier liner ~~An integrated circuit as recited in claim 1~~ wherein said barrier liner comprises

a layer of tantalum nitride,

a layer of titanium nitride, and

a layer of titanium nitride or PVD tungsten.

4. (Cancelled)

5. (Cancelled)

6. (Original) An integrated circuit as recited in claim 2 wherein said patterned aluminum layer includes a layer of at least one of titanium and titanium nitride.

7. (Original) An integrated circuit as recited in claim 3 wherein said patterned aluminum layer includes a layer of at least one of titanium and titanium nitride.

8. (Cancelled)

9. (Currently Amended) An integrated circuit as recited in claim ~~1~~ 2, further including a covering layer.

10. (Original) An integrated circuit as recited in claim 9 wherein said covering layer includes a layer of silane-based high density plasma oxide.

11. - 16. (Canceled)

17. (New) An integrated circuit as recited in claim 3, further including a covering layer.

18. (New) An integrated circuit as recited in claim 17 wherein said covering layer includes a layer of silane-based high density plasma oxide.